

WHAT IS CLAIMED IS:

1 1. A liquid crystal display comprising:  
2 a thin film transistor plate further comprising:  
3 a gate line on a first transparent substrate,  
4 a data line arranged to cross the gate line wherein the gate line is insulated  
5 from the data line,  
6 a gate electrode protruding from said gate line in an area where said data line  
7 crosses said gate line,  
8 a thin film transistor having a source electrode connected to the data line and a  
9 drain separated from the source electrode wherein the source and drain electrodes confront  
10 each other,  
11 a passivation layer covering the thin film transistor wherein a contact hole  
12 exposing a portion of the drain electrode is formed in the passivation layer, and  
13 a pixel electrode formed on the passivation layer and being connected to the  
14 drain electrode through the contact hole, wherein the pixel electrode partially overlaps the  
15 data line;  
16 a color filter plate including a black matrix, a color filter and a common electrode on a  
17 second transparent substrate; and  
18 liquid crystals injected and sealed between the thin film transistor plate and the color  
19 filter plate,  
20 wherein the black matrix of the color filter plate asymmetrically overlaps the data line

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21 of the thin film transistor plate.

1 2. The liquid crystal display according to the claim 1, wherein a location where the black  
2 matrix overlaps the data line is selected according to a direction of rubbing an alignment film.

1 3. The liquid crystal display according to the claim 1, wherein the passivation layer is an  
organic passivation layer.

4. The liquid crystal display according to the claim 3, wherein the organic passivation  
layer is made of acryl.

5. The liquid crystal display according to the claim 3, wherein the organic passivation  
layer is made of BCB.

1 6. A liquid crystal display comprising:

2 a thin film transistor plate further comprising:

3 a gate line on a first transparent substrate,

4 a first data line arranged to cross the gate line wherein the gate line is insulated  
5 from the data line,

6 a gate electrode protruding from said gate line in an area where said data line  
7 crosses said gate line,

8 a thin film transistor having a source electrode connected to the first data line

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and a drain separated from the source electrode wherein the source and drain electrodes confront each other,

a passivation layer covering the thin film transistor wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer, and

a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the first data line at a first end of the pixel electrode;

a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and

liquid crystals injected and sealed between the thin film transistor plate and the color filter plate,

wherein the pixel electrode asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end.

7. The liquid crystal display according to claim 6, wherein an overlap width between the first data line and the pixel electrode is between  $2\mu\text{m}$  and  $4\mu\text{m}$ , and wherein an overlap width between the pixel electrode and the second data line is less than  $2\mu\text{m}$ .

8. The liquid crystal display according to claim 6, wherein the overlap width between the pixel electrode and the first data line is selected according to a direction of rubbing an alignment film.

1 9. The liquid crystal display according to claim 6, wherein the passivation layer is an  
2 organic passivation layer.

1 10. A liquid crystal display comprising:

2 a thin film transistor plate further comprising:

3 a gate line on a first transparent substrate,

4 a data line arranged to cross the gate line wherein the gate line is insulated  
5 from the data line,

6 a gate electrode protruding from said gate line in an area where said data line  
7 crosses said gate line,

8 a thin film transistor having a source electrode connected to the data line and a  
9 drain separated from the source electrode wherein the source and drain electrodes confront  
10 each other;

11 a passivation layer covering the thin film transistor wherein a contact hole  
12 exposing a portion of the drain electrode is formed in the passivation layer; and

13 a pixel electrode formed on the passivation layer and being connected to the  
14 drain electrode through the contact hole, wherein the pixel electrode partially overlaps the  
15 data line;

16 a color filter plate including a black matrix, a color filter and a common electrode on a  
17 second transparent substrate; and

18 liquid crystals injected and sealed between the thin film transistor plate and the color  
19 filter plate,

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20 wherein a cut-off film is formed under the data line, said cut-off film being  
21 asymmetrically overlapped by the data line and being partially overlapped by the pixel  
22 electrode.

1 11. The liquid crystal display according to claim 10, wherein the passivation layer is an  
2 organic passivation layer.

12. The liquid crystal display according to claim 10, wherein the cut-off film and the gate  
line are formed on a same level.

13. The liquid crystal display according to claim 10, wherein an overlap region between  
the pixel electrode, the cut-off layer and the data line range has a width of between  $2\mu\text{m}$  and  
 $4\mu\text{m}$ .

1 14. The liquid crystal display according to claim 10, wherein the cut-off film is formed at  
2 one side of the data line, said side selected according to a direction of rubbing an alignment  
3 film.

1 15. A method of fabricating a liquid crystal display having a transparent substrate on  
2 which a gate line region and a data line region are defined, comprising:  
3 simultaneously forming a gate line in the gate region wherein a gate electrode  
4 protrudes from the gate line, and a cut-off film which is asymmetrically overlapped by the

5 data line region;

6 forming a data line in the data line region on the transparent substrate, wherein the  
7 data line crosses and is insulated from the gate line, and wherein a source electrode is formed  
8 at one side of the data line, and wherein a drain electrode is formed which confronts and is  
9 isolated from the source electrode;

10 forming a passivation layer covering the gate line region, the data line region and the  
cut-off film, wherein a contact hole exposing a portion of the drain electrode is formed in the  
passivation layer; and

forming a pixel electrode connected to the drain electrode through the contact hole on  
the passivation layer, wherein the pixel electrode partially overlaps the cut-off film.

16. The method according to claim 15, wherein the passivation layer is an organic  
passivation layer.

17. The method according to claim 15, wherein the cut-off film and the gate line are  
formed on a same level.

18. The method according to claim 15, an overlap region between the pixel electrode, the  
cut-off layer and the data line range has a width of between  $2\mu\text{m}$  and  $4\mu\text{m}$ .

19. The method according to claim 15, wherein the cut-off film is formed at one side of  
the data line, said side selected according to a direction of rubbing an alignment film.